

WHAT IS CLAIMED IS:

1. Branch prediction circuitry comprising:
 - a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address;
 - a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register; and
 - a selector table comprising a plurality of entries each for storing a selection bit and accessed by a pointer generated from selected bits from said branch address and bits from said history register, each said selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from said fetch-based history table.
2. The branch prediction circuitry of Claim 1 and further comprising circuitry for updating said bimodal and fetch-based branch history tables operable to:
 - set a corresponding entry in each of said bimodal and fetch-based branch history tables when a branch is taken at branch resolution time; and
 - set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time.

1 3. The branch prediction circuitry of Claim 1 and further comprising circuitry for
2 updating said selector table operable to:

3 update a selected entry in said selector table with a first value when a bimodal
4 prediction value from said bimodal branch history table correctly represents a
5 corresponding branch resolution; and

6 update a selected entry in said selector table with a second value when a
7 fetch-based prediction value from said fetch-based branch history table correctly
8 represents the corresponding branch resolution.

1 4. The branch prediction circuitry of Claim 3 wherein said circuitry for updating
2 said selector table is further operable to maintain a value in a selected entry in said
3 selector table when corresponding values from said bimodal and fetch based branch
4 history tables both correctly represent a corresponding branch resolution.

1 5. The branch prediction circuitry of Claim 3 wherein said circuitry for updating
2 said selector table is further operable to maintain a value in a selected entry in said
3 selector table when neither values from said bimodal and fetch-based branch history
4 tables correctly represent a corresponding branch resolution.

1 6. The branch prediction circuitry of Claim 3 wherein said circuitry for updating
2 said selector table is further operable to set a value in a selected entry in said selector
3 table to a value associated with said fetch-based table when corresponding values
4 from said bimodal and fetch based branch history tables both do not correctly predict
5 a corresponding branch resolution outcome.

1 7. The processing system of Claim 1 wherein said history register comprises a shift
2 register and said branch prediction circuitry further comprises circuitry for updating
3 said shift register by shifting in a preselected value in response to a prediction value
4 from a selected one of said branch history tables as selected in response to a
5 corresponding said selector bit.

1 8. A processing system comprising:
2 a first branch history table comprising a plurality of bimodally accessed entries
3 for storing a first set of branch prediction bits;
4 a second branch history table comprising a plurality of fetch-based accessed
5 entries for storing a second set of branch prediction bits;
6 a selector for selecting in response to a selection control bit selected from a set
7 of selection control bits, a bit from a selected one of said sets of bits accessed from
8 said first and second branch history tables; and
9 a selector table comprising a plurality of entries for storing said a set of selector
10 bits as a function of a performance history of said first and second sets of branch
11 prediction bits stored in said first and second branch history tables.

1 9. The processing system of Claim 8 wherein said entries of said selector table are
2 accessed using fetch-based accessing.

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2 10. The processing system of Claim 8 wherein said each said entry in said tables
comprises a 1-bit counter.

1 11. The processing system of Claim 8 wherein said first and second branch history
2 tables and said selector table form a portion of a branch execution unit.

1 12. The processing system of Claim 11 wherein said branch execution unit forms a
2 part of a microprocessor.

- 1 13. The processing system of Claim 12 and further comprising memory coupled to
2 said microprocessor.

13. The processing system of Claim 12 and further comprising memory coupled to
said microprocessor.

1 14. A method of performing branch predictions in a processing system including a
2 bimodal branch history table, a fetch-based branch history table and a selector table,
3 the method comprising the substeps of:

4 accessing the bimodal branch history table to retrieve a first branch prediction
5 bit;

6 accessing the fetch-based branch history table to retrieve a second branch
7 prediction bit;

8 selecting between the first and second branch prediction bits in response to a bit
9 retrieved from the selector table; and

10 updating the selector table as a function of actual branch resolution.

1 15. The method of Claim 14 wherein said step of updating the selector table
2 comprises the substeps of:

3 determining if the first branch prediction bit correctly predicts the branch
4 resolution outcome;

5 updating the corresponding entry in the selector table to a first logic value when
6 the first prediction bit correctly represents the branch resolution outcome;

7 determining if the second branch prediction bit correctly predicts the branch
8 resolution outcome; and

9 updating the corresponding entry in the selector table to a second logic value
10 when the second branch prediction bit correctly represents the branch resolution
11 outcome.

- 1 16. The method of Claim 15 and further comprising the steps of:
2 determining if both the first and second branch history bits correctly predict the
3 branch resolution outcome;
4 maintaining the current value in the corresponding selector table entry when
5 both the first and second branch prediction bits correctly predict the branch resolution
6 outcome;
7 determining if both the first and second branch prediction bits incorrectly
8 predict the branch resolution outcome; and
9 maintaining the current value in the corresponding selector table entry when
10 both the first and second branch history bits incorrectly predict the branch history
11 outcome.
- 12 17. The method of Claim 15 and further comprising the steps of:
13 determining whether both the first and second branch prediction bits correctly
14 predict the branch resolution outcome;
15 maintaining the current value in the corresponding selector table entry when
16 both the first and second branch prediction bits correctly predict the branch resolution
17 outcome; and
18 updating the current selector table entry to a logic value associated with the
19 fetch-based branch history table when neither the first nor second branch prediction
20 bits correctly predicts the branch resolution outcome.

1 18. The method of Claim 14 wherein said step of accessing the fetch-based branch
2 history table comprises the substep of generating an address from at least some bits of
3 a branching instruction and bits retrieved from a history register.

1 19. The method of Claim 18 wherein the history register comprises a shift register.

1 20. The method of Claim 19 wherein said method further comprises the steps of
2 updating the shift register by shifting-in the prediction bit selected by said step of
3 selecting.

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